REMARKS

This is intended as a full and complete response to the Final Office Action ("Office Action") dated July 6, 2005 having a shortened statutory period for response set to expire on October 6, 2005. Claims 1 through 20 are presently pending, and no amendments were made to the application in this Reply.

In the Office Action, text of 35 U.S.C. §103(a) is recited followed by a rejection of claims 1-20 "under 35 U.S.C. 102(a/e) as being anticipated by Dutta et al. (6,349,403) in view of Teig et al. (US 2003/0066043 A1)." Applicant has interpreted this to be an obviousness rejection in view of the combination of references and the prior reference to 35 U.S.C. §103(a). Accordingly, Applicant is reading the intent of the Office Action as being a rejection of claims 1-20 as being obvious over the cited references.

If, however, a rejection under 35 U.S.C. §102(a/e) was actually intended, Applicant respectfully requests that the rejection be immediately be withdrawn as being improper. It is well settled that an anticipation rejection cannot be based on the combination of two references. As this anticipation rejection of claims 1-20 purports to be based on the combination of two references, such rejection is improper and should be immediately withdrawn.

Assuming that the intention in the Office Action was to reject claims 1-20 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 6,349,403 B1 ("Dutta") in view of U.S. Patent Application No. 2003/0066043 A1 ("Teig"), Applicant respectfully disagrees with this rejection, at least for the reasons set forth below. In order to advance prosecution, Applicant shall initially assume *arguendo* that Dutta and Teig may properly be combined to support an obviousness argument.

At the outset, a brief description of Teig is appropriate as it is a newly cited reference in this prosecution. In Teig, a partitioning grid that divides an integrated circuit ("IC") into sub-regions is defined. Notably, this division of an IC may be "the entire IC layout, or a portion of this layout." (*See* Teig at [0091].) Moreover, this division may be for a layout of a block of an IC. (*Id.*) Teig goes on to state that either "different shaped partitioning grids" for different recursion levels may be used or

coordinates of the partitioning grid may be adjusted to match the coordinates of the IC region at the recursion level. (*See* Teig at [0104].)

Accordingly, it should be appreciated that in any implementation, the technology in Teig is wholly premised on a grid-based approach, where a grid is based on layout. Thus, it should further be appreciated that the grid in Teig is not based on circuit topology units, but rather it is layout-based.

Continuing the description of Teig, sub-regions of a partitioned region are referred to as "the current slot's child slots." (*See* Teig at [0092].) A network or "net" may include five circuit modules that are located in child slots, where more than one circuit module may be located in a child slot. (*See* Teig at [0094].) A net within a partitioning grid region is used to identify routes, which in Teig are also referred to as routing graphs or connection graphs. (*See* Teig at [0096].) Each route of a net provides a set of interconnect lines for interconnecting the child slots. (*Id.*) To model a net's configuration with reference to a grid, each child slot having a circuit module ("net's pins") is treated as a node of a routing graph. (*See* Teig at [0097].) Thus, each node may be a vertex or point of the routing graph. (*Id.*) In Teig, a Steiner tree routing graph is used. (*See* Teig at [0098].)

Accordingly, it should be appreciated that Teig is grid-based partitioning of a layout. A network, including network nodes, in sub-regions of the region partitioned is identified and may be modeled as a Steiner tree.

In the Office Action it is stated that: "Dutta et al. do not teach each of the topology units is same or similar to the other topology units." Applicant agrees with this statement. However, the next line in the Office Action states:

> Teig et al. determining routing based on assigning cost to each of routing resources, where the routing is based on Steiner trees (routing topology units), where each of the topology units is same or similar to the other topology units, because this would facilitate the placement and routing tool to explore all shortest paths between nodes of closest configuration...

With this latter statement, Applicant respectfully disagrees for at least three reasons.

First, Steiner trees are graphic models which may be applied to an integrated circuit for routing thereof. It is thus respectfully submitted that Steiner trees are not

themselves "topology units" of an integrated circuit, but rather are models for interconnecting such topology units of an integrated circuit.

Secondly, adding Steiner trees as used for gridded routing in Teig to the "gridless" routing of Dutta would not convert gridless routing of Dutta to gridded routing or something like gridded routing. Steiner trees have no apparent relevance as to whether or not grids are used, as a separate grid in Teig is defined prior to use of a Steiner tree. Thus, adding Steiner trees, if such addition were possible, to Dutta would not expand the scope of the Dutta disclosure to something more like grid-based routing.

Thirdly, even assuming *arguendo* that Steiner trees are "routing topology units," which they clearly are not, there is no basis to conclude that Steiner trees will be the same or similar to "other topology units." Even the referenced Figures 6 through 8 in Teig show three different possible outcomes using Steiner trees from routing the same set of four nodes 610, 615, 625, and 630. Moreover, in one of those possible outcomes in the Steiner tree of Figure 6 of Teig, an intermediate node, node 620, is used to obtain a possible solution, and this intermediate node does not even appear in the other two possible outcomes of Figures 7 and 8 of Teig.

In contrast to Steiner trees as referenced in Teig, Applicant's previously presented claim 1 comprises determining a respective span in terms of one or more of the topology units for each of the routing resources, wherein each of the topology units are same or similar to the other topology units. Again, for example, each tile is a region of logic and routing resources, which is replicated throughout an FPGA, which is more like grid-based routing than gridless routing as in Dutta. For at least the reasons given for claim 1, none of the independent claims 8, 12, 13, 14, 15, and 16, are described, shown, or suggested by the combination of Dutta and Teig, and thus each of such claims is allowable. Furthermore, it is respectfully submitted that claims 2-7, 9-11, and 17-20, which depend either directly or indirectly upon an allowable base claim, are likewise allowable.

Though Applicant has assumed *arguendo* in the foregoing remarks that Dutta and Teig may be combined, it is Applicant's position that these are not properly

combinable references. It is now well established that the Patent Office bears the burden of establishing a *prima facie* case to maintain a rejection for obviousness. Failure to make such a *prima facie* showing by the Patent Office is to result in a withdrawing of the rejection.

The MPEP states what the Patent Office considers to be a "*prima facie* case" of obviousness at Section 706.02(j). Taking *arguendo* the Patent Office criteria of a "*prima facie* case" of obviousness as the standard, it will become apparent that the instant rejection for obviousness fails to meet such criteria and, accordingly, that the rejection of Claims 1 through 20 for obviousness is improper and should be withdrawn.

According to the Patent Office, the first element of a *prima facie* case for obviousness is that there must be some suggestion or motivation to modify a reference or combine the teachings of the references. This suggestion must come from either of the references or be knowledge generally available to one of ordinary skill in the art.

However, there is no suggestion or motivation to modify Dutta with Teig Rather, quite the contrary. Dutta explicitly states that "gridless" cost-based routing is to be used. In complete contrast to Dutta, Teig states that a gridded form of routing is to be used. As the conceptual approaches teach away from one another, there is no suggestion or motivation to modify Dutta with Teig.

According to the Patent Office, the second element of a *prima facie* case for obviousness is that there must be a reasonable expectation of success. In the Office Action, it is argued that adding the Steiner trees of Teig to Dutta "... would facilitate the placement and routing tool to explore all shortest paths between nodes of closest configuration." However, for the below set forth reasons, the Office Action fails to meet the second element of the Patent Office's *prima facie* case for obviousness.

First, there is no mention in the Office Action of why use of a Steiner tree as in Teig would have a reasonable expectation of success in Dutta. Again, the burden is on the Patent Office to explain why there must be a reasonable expectation of success, and this burden has not been met.

Secondly, Teig is a grid-based routing technology. Accordingly, it is respectfully

submitted that these grid-based technologies do not appear to have a reasonable expectation of success, or even applicability, in the gridless-based routing of Dutta.

Thirdly, there is no indication in the Office Action of how the teachings of Dutta are to be reengineered in view of the teachings of Teig to arrive at the claimed invention. Rather, on this point, the Office Action merely has the above-quoted conclusory statement to the effect that such a reengineering would "facilitate the placement and routing tool to explore all shortest paths between nodes of closest configuration." Thus, there is no statement in the Office Action of how Dutta would be reengineered in view of Teig to arrive at the claimed invention.

According to the Patent Office, the third element of a *prima facie* case for obviousness is that the cited prior art references must teach or suggest all the claim limitations. Notably, as previously mentioned, Steiner trees are not topology units. Thus, adding Teig to Dutta fails to teach or suggest all of the limitations of Applicant's independent claims, as previously indicated.

Accordingly, it is respectfully submitted that the rejection of claims 1 through 20 under 35 U.S.C. § 103(a) as being obvious over Dutta in view of Teig is improper and should be withdrawn for any of the several reasons provided above, and it is respectfully requested that the application be passed to issuance.

Claims 1 through 20 were also rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 8 of U.S. Patent No. 6,501,297 ("Kong") in view of Teig. In response to this rejection of claims 1 through 20, Applicant has attached hereto a terminal disclaimer (completed form PTO/SB/26) to disclaim the terminal portion as set forth in such terminal disclaimer. Accordingly, Applicant respectfully requests that this rejection under the judicially created doctrine of obviousness-type double patenting of claims 1 through 20 be withdrawn and the application be passed to issuance.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 2, 2005

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